In the Claims:

1. (Previously presented) A circuit arrangement comprising: (a) a register file partitioned into a plurality of banks each bank including at least one register and at least one clock input, address input and data input; and (b) enable logic coupled to the register file and configured to selectively disable at least one unused bank from among the plurality of banks by gating off the clock, address and data inputs thereof.

2. (Original) The circuit arrangement of claim 1, wherein the each register in the register file comprises at least one of a CMOS flip flop and a CMOS latch.

3. (Previously presented) The circuit arrangement of claim 1, wherein the enable logic comprises a plurality of enable circuits each enable circuit coupled to a register bank in the register file, and each enable circuit configured to gate off each clock, address and data input supplied to the associated bank in response to a respective enable signal.

4. (Previously presented) The circuit arrangement of claim 3, wherein each enable circuit includes a plurality of gate transistors, each gate transistor coupled to one of the clock, address and data inputs, and each gate transistor responsive to the respective enable signal supplied to each enable circuit.

5. (Previously presented) The circuit arrangement of claim 1, further comprising output select logic coupled to each of the plurality of banks of registers.

6. (Previously presented) The circuit arrangement of claim 1, wherein the enable logic is configured to dynamically determine which register banks are unused and to generate an enable signal for each bank in response to the dynamic determination.

7. (Original) The circuit arrangement of claim 6, wherein the enable logic comprises an address decoder configured to generate the enable signals responsive to at least one address specified by the address inputs supplied to the register file.

8. (Original) The circuit arrangement of claim 1, wherein the enable logic is configured to generate an enable signal for each bank in response to stored power modes state information.

9. (Previously presented) The circuit arrangement of claim 8, further comprising a support register configured to store the power modes state information, wherein the support register is configured to be updated responsive to a power control instruction resident in program code being executed by a processor.

10. (Previously presented) The circuit arrangement of claim 9, wherein the support register comprises a power modes register.

11. (Previously presented) The circuit arrangement of claim 9, wherein the support register additionally stores status information that is unrelated to power dissipation control.

12. (Original) The circuit arrangement of claim 1, wherein the circuit arrangement is disposed on an integrated circuit.

13. (Original) The circuit arrangement of claim 12, wherein the circuit arrangement is disposed in a processor in the integrated circuit.

14. (Original) A program product comprising a hardware definition program defining the circuit arrangement of claim 1, and a signal bearing medium bearing the hardware definition program, wherein the signal bearing medium includes at least one of a transmission medium and a recordable medium.

15. (Original) A method of controlling power dissipation in a register file, the method comprising: (a) receiving first and second enable signals respectively directed to first and second banks of registers among a plurality of banks of registers in the register file,

wherein each bank of registers includes at least one register and at least one clock input, address input, and data input; and (b) selectively disabling the first bank of registers responsive to the first enable signal by gating off the clock, address and data inputs thereof.

16. (Original) The method of claim 15, wherein the each register in the register file comprises at least one of a CMOS flip flop and a CMOS latch.

17. (Original) The method of claim 15, wherein selectively disabling the first bank of registers includes supplying the enable signal to a plurality of gate transistors coupled to the first bank of registers, each gate transistor coupled to one of the clock, address and data inputs.

18. (Original) The method of claim 15, further comprising dynamically determining that the first bank is unused, and generating the first enable signal responsive thereto.

19. (Original) The method of claim 18, wherein dynamically determining that the first bank of registers is unused includes decoding at least one address specified by the address inputs supplied to the register file.

20. (Original) The method of claim 15, further comprising generating the first and second enable signals in response to stored power modes state information.

21. (Original) The method of claim 20, wherein the stored power modes state information is stored in a support register, the method further comprising updating the support register in response to a power control instruction resident in program code being executed by a processor.